"Applied Vertical Bloch Line Storage Technology"

R. R. Katti
Center for Space Microelectronics Technology
Jet l'repulsion I aboratory
California institute of Technology
Pasadena, California

Abstract:

Vertical Bloch Line (VBL) storage technology uniquely offers the possibility of storing data in nonvolatile, high-density, solid-state chips. For example, while semiconductor random-access memories offer high density and solid-state performance, they arc volatile; and magnetic disks offer nonvolatility and high-density but are mechanical and not solid-state. When compared to magnetic bubble devices, VBL technology offers higher storage density by reducing the dependence on bubble-to-bubble magnetostatic effects. VBL chips offer higher data rates at reduced power when compared to bubble devices by replacing the rotating in-plane field which acted on bubbles in both minor and major imps, with a gyrotropic pulse field that propagates higher mobility Bloch lines in the minor loops and with current access which acts on bubbles in the major line.

Over the past few years, a significant effort has been directed at studying and understanding the characteristics of domains, domain walls, and Bloch lines for use in VBL storage chips. It will continue to be important to study and characterize these structures statically and dynamically as storage elements, from a storage technology and computing system applications perspective. In this respect, near term and long term potential performance figures become important metr ics for VBL technology.

1 n this work, the potential performance of VBL technology has been assessed as implemented using partial grooving domain stabilization technology. The fundamental attributes of magnetic domains, domain walls, and VBLs, which can be estimated, dictate storage chip performance for applications. For example, VBL chips could achieve storage densities ranging from 1 gigabit to 1 terabit per cubic centimeter in chips with storage capacities ranging from 64 Mbits to 4 Gbits. Power levels can be expected to range approximate y from 1 to 1() mW per megabit/see of input/m tput data, and bit propagation power levels of approximately 100" mW or less per active chip. These potential performance ranges will be discussed to help evaluate the needs and role of VBL technology for storage applications.

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